TRIMMING METHOD AND TRIMMING DEVICE FOR A PLL CIRCUIT FOR TWO-
POINT MODULATION

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Cross-Reference to Related Application:

This application is a continuation of copending International

Application No. PCT/DE02/00727, filed February 20, 2002, which

designated the United States and was not published in English.

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Background of the Invention:

Field of the Invention:

The invention relates to a trimming method for a PLL (Phase

Locked Loop) circuit operating on the basis of the principle

15 of two-point modulation and also to such a PLL circuit

designed for impressing an analog and a digital modulation

signal.

A low-complexity implementation of a transmitter design for

20 transceivers in mobile radio systems is provided by

transmitters in which a PLL circuit is used as a frequency

synthesizer and is used to provide frequency modulation and

phase modulation for a radio frequency signal.

25 The modulation signal is normally impressed into the PLL

circuit using a frequency divider arranged in the PL loop's

feedback path. This involves using a digital modulation signal for continually reprogramming the digital frequency divider. This form of modulation, which is also called single-point modulation, is known in the prior art and is described in U.S.

5   Patent No. 4,965,531, U.S. Patent No. 6,008,703 and U.S. Patent No. 6,044,124, for example.

To achieve low noise in the PLL circuit, the circuit's bandwidth is designed to be much narrower than is required for

10   transmitting the modulated data. For this reason, in addition to the purely digital modulation, analog modulation is used in order to compensate for the limited bandwidth. Simultaneously impressing a digital and an analog modulation signal into a PLL circuit is called two-point modulation.

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Published German Patent Application DE 199 29 167 A1, which represents the closest prior art, describes a two-point modulator and a method for two-point phase or frequency modulation using a PLL circuit. In addition, a digital

20   modulation signal used for programming the frequency divider is converted by a digital-analog converter into an analog modulation signal that is then injected into the PL loop at a summation point situated at a suitable location. The two modulation signals are superimposed on one another at the

25   output of the PLL, and in this way a frequency-independent transfer response is obtained for the loop.

One difficulty with two-point modulation is that, besides the inphase synchronization, a high level of concurrence among the amplitudes of the two modulation signals used is required.

5 Because of production tolerances in the components for analog modulation, however, variations always arise in the modulation gradient and in the modulation's amplitude level. For this reason, it is necessary to perform amplitude trimming between the analog and the digital modulation following production of

10 the PLL circuit.

If it is additionally necessary to take into account temperature influences as well, such trimming needs to be performed again before every transmission operation.

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A known method for trimming a PLL circuit involves impressing the two-point modulation on the circuit in the locked state and using an external test receiver to receive the transmitted signal, to demodulate it and to trim the digital and analog

20 modulation signals on the basis of the demodulation result. On account of the nonlinear response of the element which produces oscillations (this is a voltage-controlled oscillator or VCO) in the PLL circuit with regard to the frequency as a function of the control voltage, this trimming needs to be

25 performed for every channel, however, which, when there are a large number of channels, means a test period of corresponding

length. In addition, the trimming information needs to be stored in a memory, and another drawback is that the influence of temperature changes is not taken into account in this method.

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Another option is to receive and demodulate the signal produced by the PLL circuit using the reception part of the transceiver. However, this would require a complete second PLL circuit in the receiver, which significantly increases the

10 circuit complexity disadvantageously.

Summary of the Invention:

It is accordingly an object of the invention to provide a PLL circuit designed for impressing an analog modulation signal

15 and a digital modulation signal based on a two-point modulation and to provide a trimming method for a PLL circuit operating based on the principle of two-point modulation, which overcome the above-mentioned disadvantages of the prior art apparatus and methods of this general type.

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In particular, an object of the invention to provide a trimming method for a PLL circuit operating on the basis of the principle of two-point modulation which allows rapid amplitude trimming with little complexity and which permits

25 temperature influences to be taken into account. The object of the invention is also to provide a PLL circuit having a

trimming unit that can be implemented with little complexity
and that allows the amplitude of the modulation signals to be
trimmed quickly and without any problems.

5   With the foregoing and other objects in view there is
provided, in accordance with the invention, a method for
amplitude trimming between an analog modulation signal and a
digital modulation signal for a PLL circuit operating based on
a two-point modulation. The method includes initially
10   operating the PLL circuit without impressing any modulation,
i.e. the PLL circuit is locked to a desired frequency. Next,
an analog and a digital modulation signal are impressed into
the locked PLL circuit. Provided that these signals do not
have identical amplitudes (in this case, the modulation swings
15   would already have been trimmed), this results in a PLL
control error. A signal that is characteristic of the PLL
control error is then tapped from the PLL circuit. The
modulation swing in the analog modulation signal is then
changed such that the signal that is characteristic of the PLL
20   control error has the same value as before the analog and
digital modulation signals were impressed.

With this type of trimming, the output signal produced by the
PLL circuit is not demodulated, because trimming involves
25   reverting to the signal that is characteristic of the control
error in the PLL circuit. Accordingly, it is not necessary to

provide an internal or external demodulator, which keeps down
circuit complexity and achieves a high level of practicability
for the inventive trimming method.

5   One advantageous exemplary embodiment of the inventive method
is characterized in that the signal that is characteristic of
the control error in the PLL circuit is a voltage signal that
is tapped from the PLL circuit via a charge pump and a low-
pass filter. By virtue of a suitable design for these
10   components, it is possible to achieve a sufficiently high
level of sensitivity for the trimming method.

To change the modulation swing in the analog modulation
signal, the following steps are preferably carried out: the
15   signal that is characteristic of the control error is compared
with a reference signal having a fixed value, thus producing a
comparison signal. The comparison signal is evaluated before
and after the analog and digital modulation is impressed. The
modulation swing in the analog modulation signal is changed on
20   the basis of the evaluation result.

One advantageous exemplary embodiment of the inventive method
is characterized in that the reference signal is provided by
adjusting (i.e. programming) the PLL circuit in the
25   deactivated state to a desired channel center frequency,
activating the PLL circuit and thereby locking it, and

producing the reference signal from the signal that is characteristic of the control error in the PLL circuit during the locking process. In this exemplary embodiment, the reference signal required for trimming is to a certain extent

5   produced using the PLL circuit itself.

An alternative exemplary embodiment, which is likewise advantageous, is characterized in that a prescribed reference signal is provided externally. The prescribed reference signal

10 can be identical for all channel center frequencies, or it is also possible to provide a reference signal that is dependent on the desired channel center frequency.

The inventive PLL circuit has an associated trimming unit

15 which includes a device for tapping a signal that is characteristic of the PLL control error from the PLL circuit and also a device for evaluating the signal that is characteristic of the control error and also a device for changing the modulation swing in the analog modulation signal

20 on the basis of the evaluation result.

An inexpensive implementation, using simple circuitry, of the device for tapping the signal that is characteristic of the PLL control error from the PLL circuit includes a charge pump

25 and a low-pass filter which is connected downstream of the charge pump.

The device for evaluating the characteristic signal preferably

includes a device for comparing the signal that is

characteristic of the control error with a reference signal

5   having a fixed value, thus producing a comparison signal, and

a device for evaluating the comparison signal before and after

the analog and digital modulation is impressed. In this case,

the reference signal should be chosen such that the comparison

device (comparator) is operated in the range of maximum

10   sensitivity.

Other features which are considered as characteristic for the

invention are set forth in the appended claims.

15   Although the invention is illustrated and described herein as

embodied in a trimming method and trimming device for a PLL

circuit for two-point modulation, it is nevertheless not

intended to be limited to the details shown, since various

modifications and structural changes may be made therein

20   without departing from the spirit of the invention and within

the scope and range of equivalents of the claims.

The construction and method of operation of the invention,

however, together with additional objects and advantages

25   thereof will be best understood from the following description

of specific embodiments when read in connection with the

accompanying drawings.

Brief Description of the Drawings:

5   Fig. 1 is a block diagram of a PLL circuit arrangement which

operates on the basis of the principle of two-point modulation

and has a trimming unit in accordance with the invention;

Fig. 2 is a block diagram of a first exemplary embodiment of

10   the trimming unit shown in Fig. 1;

Fig. 3 is a block diagram of a second exemplary embodiment of

the trimming unit shown in Fig. 1;

15   Fig. 4 is a block diagram of a charge pump used in the

trimming unit; and

Fig. 5 is a block diagram of a circuit diagram of a low-pass

filter used in the trimming unit.

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Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and

first, particularly, to Fig. 1 thereof, there is shown a PLL

circuit 10 which operates on the basis of the principle of

25   two-point modulation and is coupled to a trimming unit 30.

In line with an ordinary design, the signal path of the PLL

circuit 10 has a phase detector PFD (Phase Frequency Detector)

12, a charge pump CP 24, a loop filter LF 14, a summation

point 15 and a voltage-controlled oscillator VCO 16.

5

The VCO 16 is the element that produces oscillations in the

PLL circuit 10 and delivers a signal of frequency F_{OUT} as the

output signal from the PLL circuit 10.

10   The PLL control loop 10 is closed by a feedback path that

returns the output signal from the VCO 16 to the frequency

detector 12 via a programmable frequency divider DIV 18.

The action of the PLL circuit as a frequency synthesizer for

15   two-point modulation is known. Two-point modulation involves

impressing a digital and an analog modulation signal on the

PLL circuit 10. Fig. 1 shows an example of a modulation

circuit 11 that is used to condition the two modulation

signals and to supply them to the PLL circuit 10. The

20   modulation circuit 11 shown here, by way of example, includes

a programming device 20 and a digital-analog converter DAC 22.

A modulation signal is added to a carrier signal, forming the

basis of the PLL frequency synthesis, at a summation point 19,

and the resultant added signal 21 is supplied to the

25   programming device 20. In addition, the modulation signal is

also supplied to the digital-analog converter 22.

The programming device 20, which can be a programming device 20 containing a sigma-delta modulator, for example, produces a control signal 23 that is supplied to the programmable

5   frequency divider 18. The control signal 23 is a digital signal that specifies a division ratio 1:N. N is an integer and is subject to constant changes on account of the modulation signal, as a result of which the programmable frequency divider 18 is continually reprogrammed. The

10   continual reprogramming of the frequency divider 18 impresses the digital modulation into the PLL circuit 10.

The frequency divider 18 can be a "fractional-N frequency divider", for example. Fractional-N frequency dividers allow

15   frequency division by nonintegers also ("fractional synthesis technique"). The fractional synthesis technique is advantageous because the interference arising in the case of integer division as a result of lateral lines in the spectrum of the output signal are avoided.

20

Analog modulation is performed using the digital-analog converter 22 and the summation point 15. The digital-analog converter 22 produces an analog output signal that is superimposed on the control signal for the VCO 16 by the

25   summation point 15.

It will be pointed out that the modulation circuit 11 can also be implemented in another way. By way of example, when an analog modulation signal is used, the digital-analog converter 22 can be dispensed with and instead a corresponding signal

5   conversion can be performed in the digital modulation path. The only point of significance to the invention is that, for the two-point modulation, one of the modulation signals is an analog signal and the other modulation signal is a digital signal.

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The way in which the PLL circuit works in the locked state is known and is explained briefly below:

The frequency divider DIV 18 outputs a frequency divider

15   signal 13 that is produced from the output signal from the PLL circuit 10 in the manner already described by frequency division. The phase detector PFD 12 compares the phases with the two signals obtained and produces a control signal 17 that corresponds to the phase difference between the two signals

20   obtained. The control signal 17 is used to actuate the charge pump CP 24. A current generated in the charge pump 24 on the basis of the control signal 17 is used to charge the loop filter LF 14. Since the loop filter LF 14 is a low-pass filter, signal components of relatively high frequency are

25   smoothed in this manner. The output of the loop filter LF 14

is then used, after the addition of the analog modulation at the summation point 15, to control the oscillator 16.

Since the analog modulation signal is subject to drift and
5   tolerances, unlike the digital modulation signal 23, which has no tolerances on account of its discrete nature, it is necessary to make the amplitudes of the two modulation signals more alike. For this purpose, the PLL circuit 10 is coupled to a trimming unit 30, whose operation and design will be
10   explained in more detail below. The trimming unit 30 outputs a control signal 31 that is supplied to an amplitude influencing device 32 for influencing the amplitude of the analog modulation signal.

15   To give a better understanding, the principle of action of the two-point modulation technique will be explained briefly: during operation, impressing the modulation into the PLL control loop 12, 24, 14, 16, 18 must not involve any reaction to the modulation by the closed control loop. This is achieved
20   by virtue of the analog modulation, which is impressed in analog form at the summation point 15, being compensated for by a correspondingly opposite change in the division factors of the frequency divider 18, prompted by the digital modulation. Hence, if the analog modulation increases the
25   output frequency F_{OUT} from the VCO, then the division factor simultaneously needs to be increased to the same extent (by

the digital modulation), so that the output frequency from the
frequency divider 18 (the frequency divider signal 13) remains
unchanged by the modulation. Similarly, if the output
frequency F_{OUT} is lowered, the division factor needs to be
5   lowered accordingly. That is to say that, if the analog and
digital modulation swings concur exactly, the closed loop
behaves like an open loop.

If the modulation swings do not concur, then the PLL control
10   loop corrects the error. A measure of the inequality of the
modulation swings is the voltage change which appears at the
output of the loop filter LF 14 when the modulations are
added. This voltage change is generally very small (a few mV),
however. The invention is now based on the idea of using a
15   parallel path to the same effect to make this voltage change
available in an order of magnitude that is easier to evaluate
(e.g. several 100 mV). In this case, the same conditions
apply: no control action in the PLL control loop means no
activity on the phase detector PFD 12 and hence no voltage
20   change at the output of the parallel path.

Fig. 2 shows a first exemplary embodiment of the inventive
trimming unit 30. The trimming unit 30 includes a second
charge pump CP2 33 and a second low-pass filter LF2 34, which
25   is connected downstream of the second charge pump CP2. The
second charge pump LF2 34 and the second low-pass filter 34

-14-

produce the parallel path mentioned above. The output of the

low-pass filter LF2 34 is supplied to one of the inputs of a

comparator 35. The other input of the comparator 35 is

connected to the output of a buffer 36. A capacitor 37 is

5   situated between the second comparator input and ground. An

output of the comparator 35 is supplied to an evaluation

circuit 38 which produces the control signal 31.

The inventive trimming unit 30 is used in the following manner

10   to trim the modulation amplitudes:

First, the PLL circuit 10 is programmed to the desired channel

center frequency before the transmission operation. This is

done merely by adjusting the appropriate division factor N or

15   the digital channel representation (e.g. a channel word when

using a fractional-N sigma-delta programmer 20) on the

frequency divider 18.

When the desired channel center frequency has been set, the

20   PLL circuit 10 is turned on and locks onto the channel center

frequency.

While the PLL circuit 10 is locking, the second low-pass

filter LF2 34 is charged via the second charge pump CP2 33. A

25   switch 39 which is closed during the locking process is used

to supply the output signal from LF2 34 to the buffer 36. This

involves the capacitor 37 arranged at the output of the buffer
36 being charged.

The charging of the capacitor 37 serves to produce a reference
5   signal. When the PLL circuit 10 has locked, the switch 39 is
opened. The result of this is that the voltage produced by
charging the capacitor 37 is now applied to the second input
of the comparator 35 as a constant reference voltage V_{REF}.

10   Next, a constant modulation (i.e. a "DC voltage test
modulation") is impressed both in analog and in digital form
for a particular period. As a result of the aforementioned
amplitude error in the analog modulation (i.e. as a result of
the erroneous analog modulation swing as compared with the
15   digital modulation swing), the voltage which is output by the
second low-pass filter LF2 will now change accordingly. The
voltage at the output of the second low-pass filter LF2 is
compared with the reference voltage in the comparator 35, and
the comparison result is continually communicated to the
20   evaluation circuit 38. The evaluation circuit 38 evaluates the
comparison signal obtained from the comparator 35 and, in so
doing, detects a change in the voltage which is output by the
second low-pass filter LF2 (i.e. the evaluation circuit 38
compares the comparator comparison signal obtained following
25   locking of the PLL but before the analog and digital
modulations are applied with the comparator comparison signal

obtained after the analog and digital modulations have been applied). The control signal 31 produced by the evaluation circuit 38 then uses the device 32 to prompt a change in the amplitude of the analog modulation swing or in the analog

5   modulation signal such that the voltage difference appearing at the output of the second low-pass filter LF2 34 with respect to the voltage obtained in the preceding step (with no modulation) is eliminated.

10   The signal that is output by the comparator 35 can be evaluated in the evaluation circuit 38 using an iterative process. For example, i.e. the analog modulation amplitudes · are approximately trimmed step by step with alternately updating the control signal 31 and assessing the resultant,

15   changed output signal from the comparator 35. When the voltage change at the output of the low-pass filter LF2 has been eliminated, which voltage change occurred when the analog and digital modulations were added, the digital and analog modulation swings have been aligned.

20

Fig. 3 shows a second exemplary embodiment of the trimming unit 30. Components that are the same or have the same function have been denoted using the same references as in Fig. 2. The trimming unit 30 again includes a second charge

25   pump CP2 33, a second low-pass filter LF2 34, a comparator 35 and an evaluation circuit 38. In respect of these components,

the circuit design of the second exemplary embodiment is identical to the circuit design of the first exemplary embodiment shown in Fig. 2. In addition, the circuit has a node 40 via which a prescribed external, fixed reference

5 voltage V_{REF} can be applied to the second comparator input. The external reference voltage V_{REF} can also be applied to the input of the second low-pass filter LF2 34 via a switch 39'.

The circuit shown in Fig. 3 differs from the circuit shown in

10 Fig. 2 essentially only in that the reference voltage for the comparator 35 is in this case not derived from the PLL's locking process but rather is produced externally. The modulation swing is trimmed in the following manner:

15 Either before the PLL circuit 10 is turned on or when the PLL circuit 10 has already been turned on and has locked, the second charge pump CP2 33 is deactivated and the switch 39' is closed. The result of this is that the second low-pass filter LF2 34 is charged solely using the reference voltage V_{REF}

20 (precharging), since the second charge pump CP2 33 has a high impedance in the deactivated state. The evaluation circuit 30 is thus decoupled from the PLL circuit 10 in this state.

Following charging of the low-pass filter LF2 34, setting of

25 the channel center frequency and the locking process in the PLL circuit 10, which leaves the trimming unit 30 unaffected

in this case, the switch 39' is opened. This fixes the reference voltage V_{REF} applied to the second input of the comparator 35 (at least for the duration of the subsequent trimming). Next, the second charge pump CP2 33 is activated.

5   The rest of the procedure corresponds to the method already explained with reference to Fig. 2 (impressing the constant analog and digital modulations, trimming the voltage difference arising in the process at the output of the low-pass filter 34 using the evaluation circuit 38 and the device

10   32 for influencing the amplitude of the analog modulation signal).

   Both exemplary embodiments allow the constant reference voltage required at the second comparator input to be produced

15   with little complexity and in a power-saving manner. In the second exemplary embodiment, the reference voltage used can be the supply or bandgap voltage which is present anyway, for example. In this case, the reference voltage should be in the range of maximum sensitivity of the comparator 35 as far as

20   possible.

Fig. 4 shows one possible implementation of the second charge pump CP2 33. The second charge pump CP2 33 includes two controllable current sources 33.1 and 33.2 which are connected

25   in series between an operating voltage V_S and ground. The two controllable current sources 33.1, 33.2 are usually single

transistors or multi-transistor circuits. The current sources 33.1, 33.2 are controllable by means of an input signal which in the present case is the control signal 17 provided by the control error in the PLL circuit. The charge pump can also be

5 actuated by providing two control signals ("up" and "down" signals) which are output directly by a phase detector of appropriate design. The output of the second charge pump 33 shown in this case branches off at the connection between the two current sources 33.1 and 33.2.

10

Fig. 5 shows a circuit example for the second low-pass filter LF2 34. As in the circuit example shown in Fig. 4, it is possible to use a multiplicity of other circuits.

15 The low-pass filter 34 includes three capacitors 34.1, 34.2 and 34.3 which - in the case of the capacitor 34.2 via a resistor 34.4 - can be charged via the filter input. The signal path contains a resistor 34.5.

20 In summary, it can be stated that the two exemplary embodiments are largely comparable up to the feature of providing the reference voltage V_{REF}, and their common action is based on the fact that, in the event of an amplitude difference between the two modulations, the phase detector PFD

25 12 establishes a control error which is picked up by the

trimming unit 30, is conditioned in a suitable manner and is utilized for amplitude trimming.